



US 09/945512

PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes Examiner: Richard Booth  
Serial No.: 09/945512 Group Art Unit: 2812  
Filed: August 30, 2001 Docket: 1303.027US1  
Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL  
BARRIER INTERPOLY INSULATORS

---

COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Mail Stop RCE  
Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

| <u>Serial No.</u> | <u>Filing Date</u> | <u>Attorney Docket</u> | <u>Title</u>   |
|-------------------|--------------------|------------------------|--|
| 09/945507         | August 30, 2001    | 1303.014US1            | FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS                                    |
| 09/945395         | August 30, 2001    | 1303.019US1            | DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS      |
| 09/943134         | August 30, 2001    | 1303.020US1            | PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS                 |
| 09/945498         | August 30, 2001    | 1303.024US1            | INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD  |
| 09/945554         | August 30, 2001    | 1303.028US1            | SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS      |
| 09/945500         | August 30, 2001    | 1303.029US1            | PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS |

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/945512

Filing Date: August 30, 2001

Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Page 2

Dkt: 1303.027US1

|           |                   |             |  |
|-----------|-------------------|-------------|--|
| 10/028001 | December 20, 2001 | 1303.035US1 | PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS         |
| 10/081818 | February 20, 2002 | 1303.045US1 | ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS |
| 10/177096 | June 21, 2002     | 1303.063US1 | GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS                                 |



Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 349-9587

Date

17 Sept '03

By

Timothy B. Clise

Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 17th day of September, 2003.

Name

Amy Moriarty

Signature

Amy Moriarty